		status pin (LAST) thus allowing the user to determine whether there is a reserve sound switching capability when the decoder is out of sync or receiving' trasparent data'. RSSF is signal which indicates the reserve sound switching status. When high, this output shows that the conventional analogue FM signal is the same as the digital signal being decoed. Thus a failure of the digital signal can result in the switching to the conventional analogue sound.

VDSP	RSSF	FLO	LAST	
0	X	X	0	
1	0	0	0	Where "X" denotes
1	1	0	1	"don't care"
1	X	1	1	

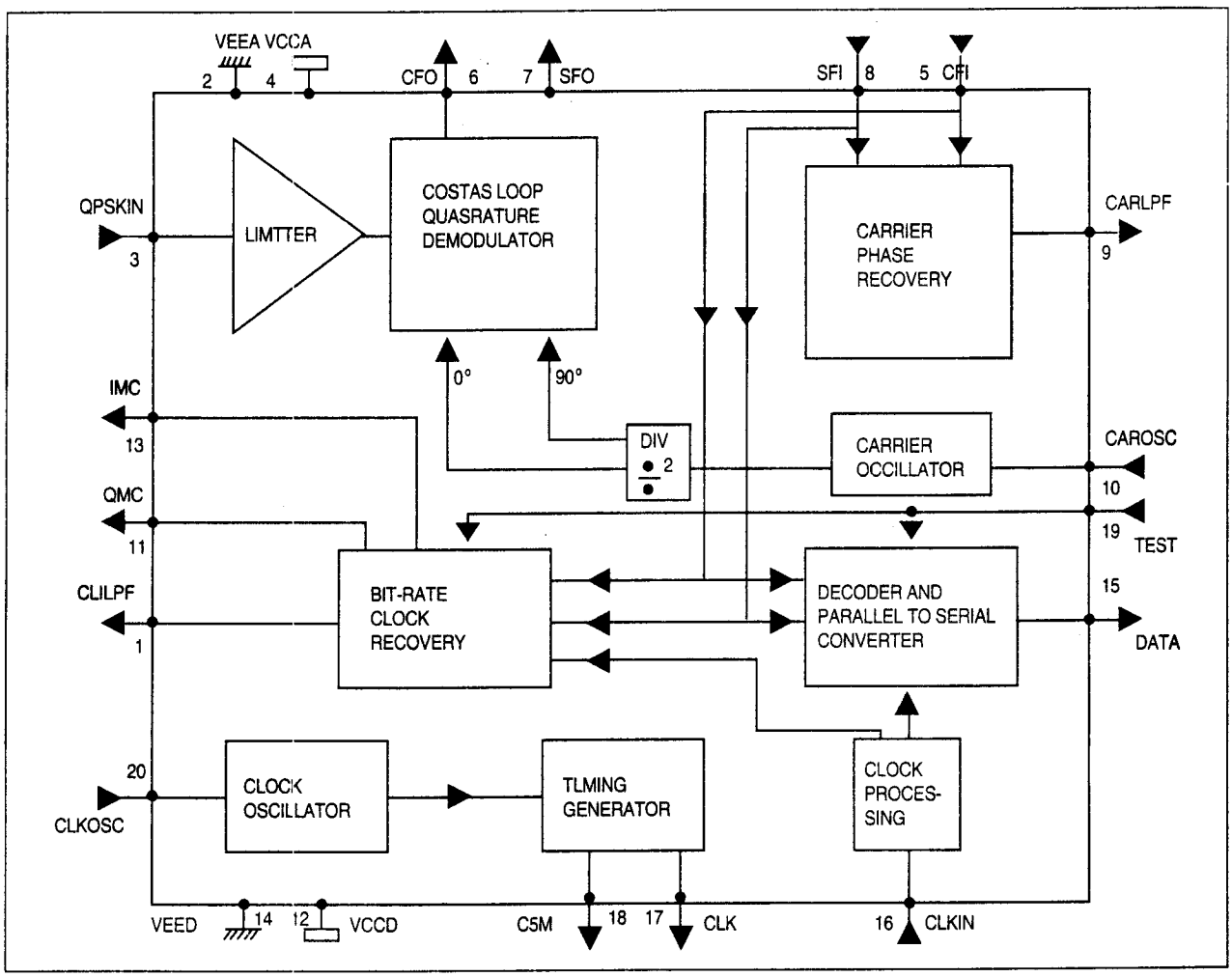
23	$\overline{CFC}$	Active low open drain output. Signals a configuration change at the 16-frame boundary (not 8ms in advance). It is cleared by a status register read in I²C or after 128ms time out for non-I²C applications.
24	SDA	I²C data input/open drain output.
26	SCL	I²C clock input. (Maximum speed 100KHz).
27	D/$\overline{S}$	Output pin which indicates whether single or dual mono sound signals are being trasmitted, D/$\overline{S}$=1 indicates dual mono, D/$\overline{S}$=0 indicates not dual mono. This bit is also available within the I²C register map.
28	S/$\overline{M}$	Output pin which indicates whether stereo or mono sound is being transmitted. S/$\overline{M}$=1 indicates stereo, S/$\overline{M}$=0 indicates mono. This bit is also available within the I²C register map.

16. TDA 8732 (Nicam Demodulator)

(1) Features

- 5V supplies for analog and digital circuitry
- Limiting amplifier for QPSK input
- Suitable for PAL B/G and PAL I NICAM-728 system.

(2) Block Diagram



(3) Pin Description

Pin No.	Symbol	Description
1	CLKLPF	Transconductance output for bit-rate loop low-pass filter
2	VEEA	Ground for analog circuitry
3	QPSKIN	QPSK modulated data input
4	VCCA	Power supply for analog circuitry
5	CFI	Baseband cosine channel input after filtering
6	CFO	Demodulated cosine channel output to low pass filter
7	SFO	Demodulated sine channel output to low pass filter
8	SFI	Baseband sine channel input after filtering
9	CARLPF	Transconductance output for carrier loop low-pass filter
10	CAROSC	Xtal input for carrier oscillator (frequency is 11.7 MHz or 13.104 MHz)
11	QMC	Monostable components connection for quadrature data transition detector
12	VCCD	Power supply for digital circuitry
13	IMC	Monostabel components connection for in-phase data transition detector
14	VEED	Ground for digital circuitry
15	DATA	728 kbit/s demodulated and differentially decoded serial data output
16	CLKIN	Bit-rate clock input at 728 KHz, phase-locked to the data
17	CLK	Output clock frequency at 728KHz
18	C5M	Reference frequency output at 5.824 MHz
19	TEST	Input for test purpose (grounded for normal operation)
20	CLKOSC	Xtal input for clock oscillator (frequency is 11.648 MHz)

17. HY6264 (KM6264AL) (8K × 8-Bit Static RAM)

(1) Decription

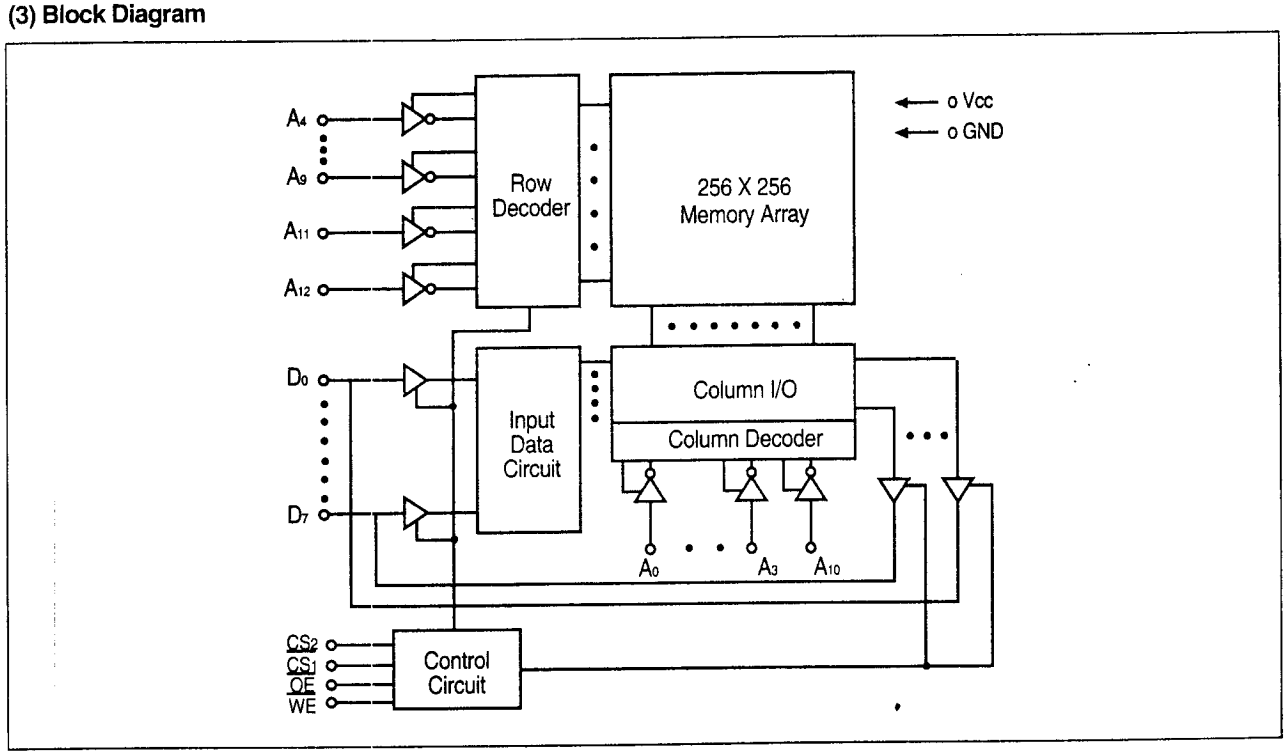
The HT6264/L is a high speed, low power, 8,192-word by 8-bit CMOS static RAM fabricated using high-performance CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields access times of 85ns maximum.

The HY6264L has a data retention mode that guarantees data will remain valid at a minimum power supply voltage of 2.0 volts. Using CMOS technology, supply voltages from 2.0 to 5.5 volts have littie effect on supply current in data retention mode.Reducing the supply voltage to minimize current drain is unnecessary with the HY6264/L family.

(2) Features

- High speed-85/100/120/150 ns (Max)
- Low power
  - 250 mW typical operating
  - 10 µW typical standby (HY6264L)
  - 10 µW typical data retention (HY6264L)
- Battery Back up (HY6264L)
  - 2 Volts data retention
- Fully static operation
  - No clock or refresh required
- All inputs and outputs directly TTL compatible
- Tri-State Outputs
- High reliability 28-pin 600 mil P-DIP and 340 mil SOP

(3) Block Diagram



(4) Pin Description

A0 - - A12	Address Input
D0-D7	Data Input/Output
CS1	Chip Select One
CS2	Chip Select Two
WE	Write Enable
OE	Output Enable
Vcc	Power
GND	Ground

18. SAA 5246 (Intergrated VIP and Teletext (IVT))

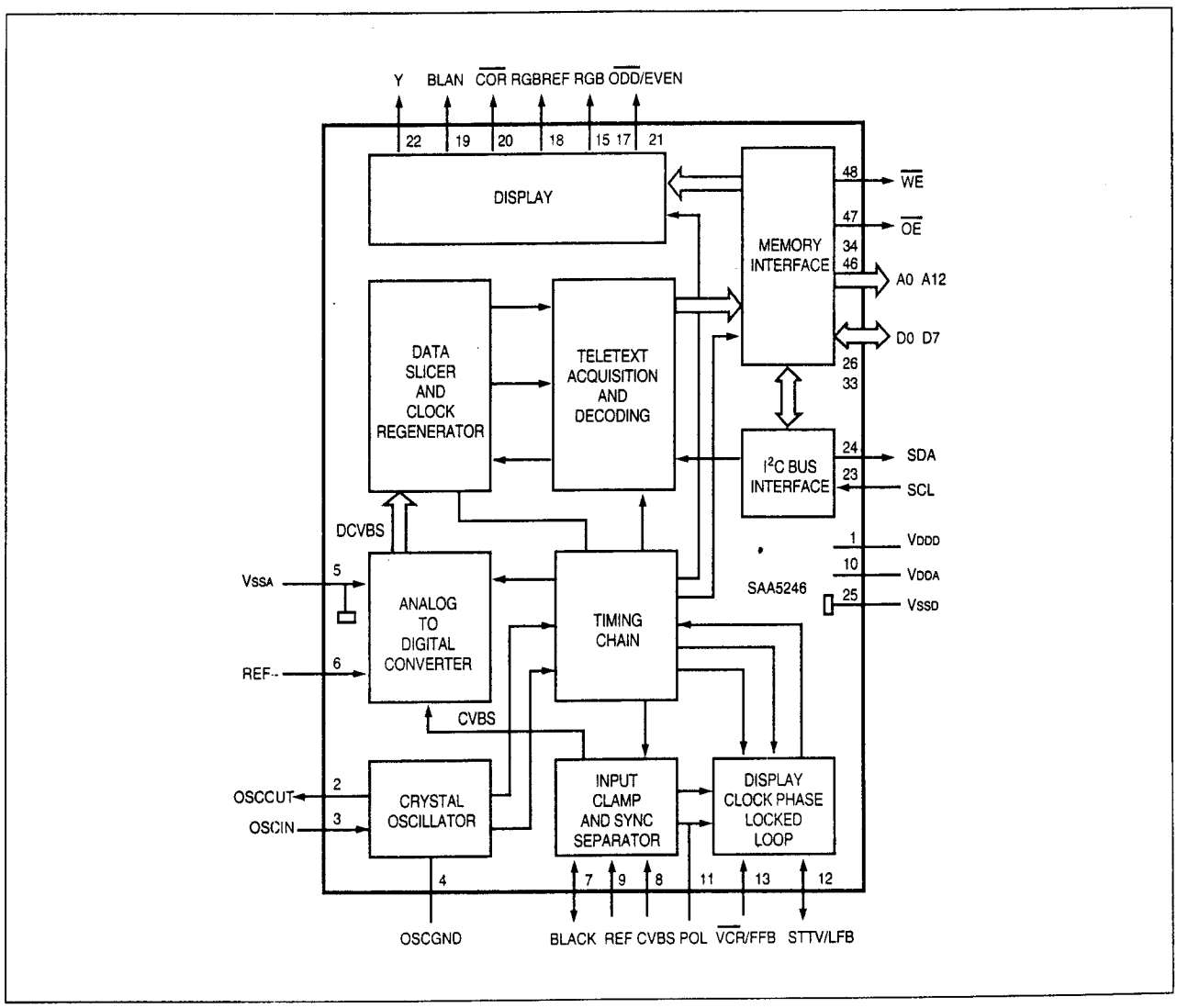
(1) General Description

The integrated VIP and Teletext (IVT) is a teletext decoder (contained within a single chip package) for decoding 625-line based World System Teletext transmissions. The teletext decoder hardware is based on the Enhanced Computer Controlled Teletext (ECCT) device (SAA5243) with some additional features; existing ECCT software remains compatible.The Video Input Processor (VIP) section of the device uses mixed analog and digital designs for the data slicer and the display clock phase-locked loop functions. As a result the number of external components is greatly reduced and no critical or adjustable components are required.

(2) Features

- Complete teletext decoder in a sinlge package
- Single +5V power supply
- Digital data slicer and display clock phase-locked loop reduce peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- 4/8 page acquisition system is software compatible with ECCT
- RGB interface to standard colour decoder ICs, push-pull output drive; requires only 2 external resistors
- Data capture performance comparable with SAA5231 (VIP2)
- Software compatibility with ECCT maintained
- Interfaces with 8K × 8-bit static RAM
- Optional storage of packer 24 in the display memory
- Packet 8/30/2 mapped to a different extenion chapter, as an aid for VCR programming applications
- Automatic ODD/EVEN output control
- Control of display PLL free-run and rolling header via I²C-bus
- Software readable ROM version national option

(3) Block Diagram



(4) Pin Description

Pin No.	Symbol	Description
1	V_{DD}	+5V supply to digital sections of the device.
2	OSCOUT	27 MHz crystal oscillator output.
3	OSCIN	27 MHz crystal oscillator input.
4	OSCGND	0V crystal oscillator ground.
5	V_{SSA}	0 V analog ground.
6	RFE+	Positive reference voltage for the ADC. The pin should be connected to analog +5V.
7	BLACK	Video black level storage pin, connected to analog ground via a 100 nF capacitor.
8	CVBS	Composite video input pin. A positive-going 1V (peak-to-peak) input is required, connected via a 100 nF capacitor.
9	IREF	Reference current input pin, connected to analog ground via a 27kΩ resistor.
10	V_{DDA}	+5V supply to the analog sections of the device.
11	POL	STTV/LFB/FFB polarity selection pin.
12	STTV/LFB	Sync to TV output pin/line flyback input pin. Fuction controlled by an internal register bit (scan sync mode).
13	VCR/FFB	PPL time constant switch/field input pin. Fuction controlled by an internal register bit (scan sync mode).
14	V_{SSD}	Connected to V_{SSD} for normal operation.
15	R	Dot rate character output of the RED colour information.
16	G	Dot rate character output of the GREEN colour information.
17	B	Dot rate character output of the BLUE colour information.
18	RGB REF	Input DC voltage to define the output high level on the RGB pins.
19	BLAN	Dot rate fast blanking output.
20	COR	Programable output to provide contrast reduction of the TV picture for mixed test and picture displays or when viewing news flash/subtitle pages. Open drain output.
21	ODD/EVEN	25 Hz output synchronized with the CVBS input's field sync pulses to produce a noninterlaced display by adjustment of the vertical deflection currents.
22	Y	Dot rate character output of teletext foreground colour information. Open drain output.
23	SCL	Serial clock input for I²C-bus. Open drain output. It can still be driven during power-down of the device.
24	SDA	Serial data port for the I²C-bus. Open drain output. It can still be driven during power-down of the device.
25	V_{SSD}	0V digital ground.
26-33	D0-D7	Data lines for the page RAM.
34-46	A0-A12	Address lines for the page RAM.
47	OE	Output enable to the page RAM.
48	WE	Write enable to the page RAM

19. MAB 8461/PCF84C81 (Single-Chip 8-Bit Microcontroller)

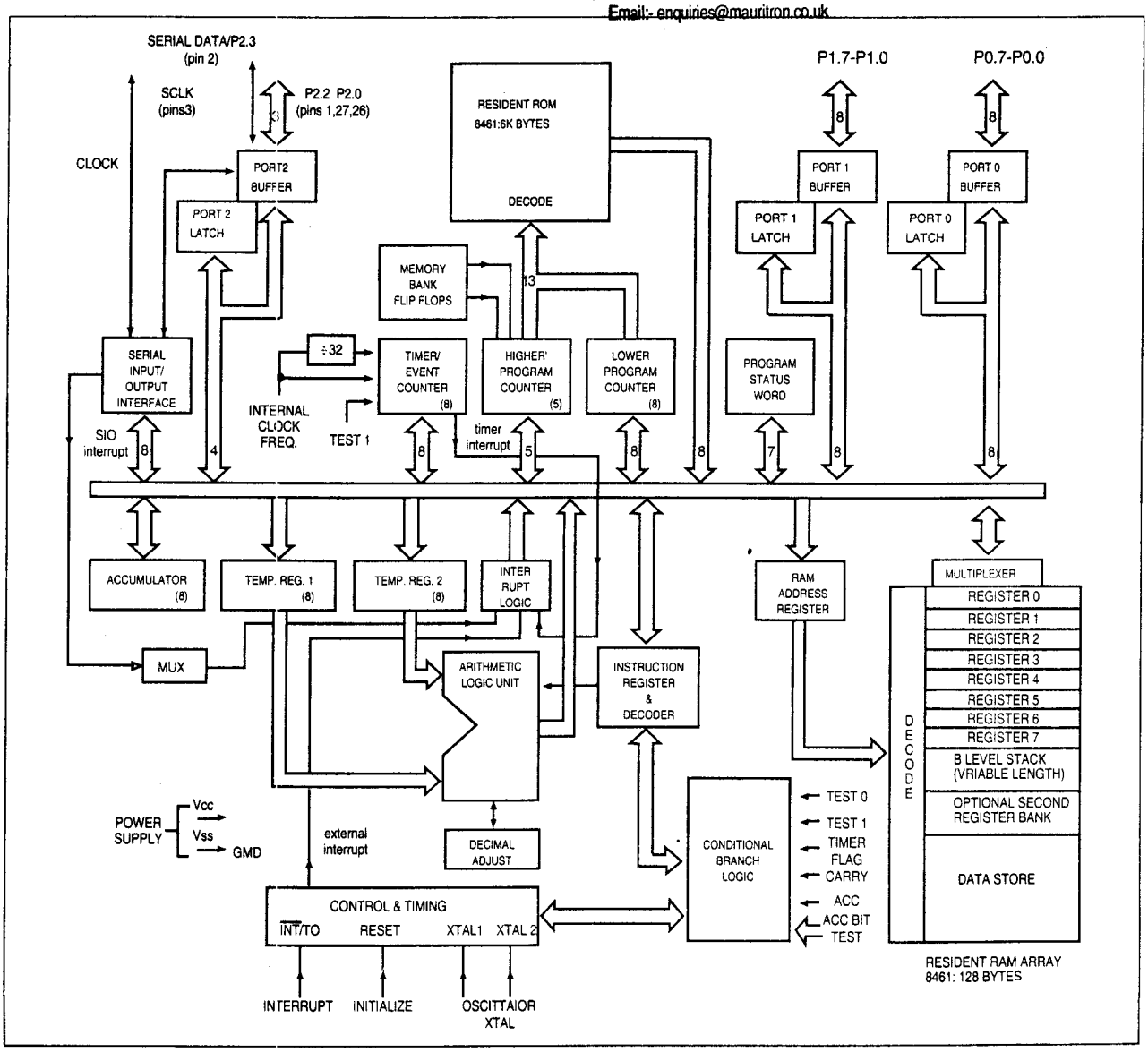
(1) Description

The MAB84X1 family of microcontrollers is fabricated in NMOS.
And PCF84C81 is fabricated in CMOS.
Each version has 20 quasi-bidirectiona I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer/event counter and on-board clock oscillator and clock circuits.
This microcontroller family is designed to be an efficient controller as well as an arithmetic processor.
The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

(2) Feautures

- 8-bit CPU, ROM, RAM and I/O in a single 28-lead DIL package
- 6K ROM bytes (MAB8461), 8K×8 ROM (PCF 84C81)
- 128 RAM bytes (MAB8461), 256×8 RAM (PCF84C81)
- 20 quasi-bidirectional I/O port lines
- Two testable inputs: one of which can be used to detect zero cross-over, the other is also the external interrupt input
- Single level vectored interrupts: external, timer/even counter, serial I/O
- Serial I/O that can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single 5V power supply (±10%)
- Operating temperature ranges: 0 to +70℃ (MAB8461)
  -40 to +85℃(PCF84C81)

(3) Block Diagram



(4) Pin Description

Pin No.	Symbol	Description
3	SCLK	Clock: bidirectional clock for serial I/O
4-11	P0.0-P0.7	Port 0: 8-bit quasi-bidirectional I/O port.
12	INT/T0	Interrupt/Test 0: external interrupt input (negative edge triggedred)/test input pin; when used as a test input, this pin is directly tested by conditional branch instursions JT0 and JNT0.
13	T1	Test 1: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the START CNT instruction.
14	Vss	Ground: circuit earth potential.
15	XTAL 1	Oscillator input: input from a crystal which determines the internal oscillator frequency or an external clock generator.
16	XTAL 2	Oscillator output : output of the inverting amplifier.
17	RESET	Reset input: used to initialize the microcontroller (active HIGH); also output of power on-reset circuit.
18-25	P1.0-P1.7	Port 1: 8bit quasi-bidirectional I/O port.
26, 27, 1, 2	P1.0-P2.3	Port 2: 4bit quasi-bidirectional I/O port. P2.3 is the serial data input/output in serial I/O mode.
28	V_{DD}	Power supply: 2.5V to 5.5V

20. SAA 3010 (Infrared Remote Control Transmitter RC-5)

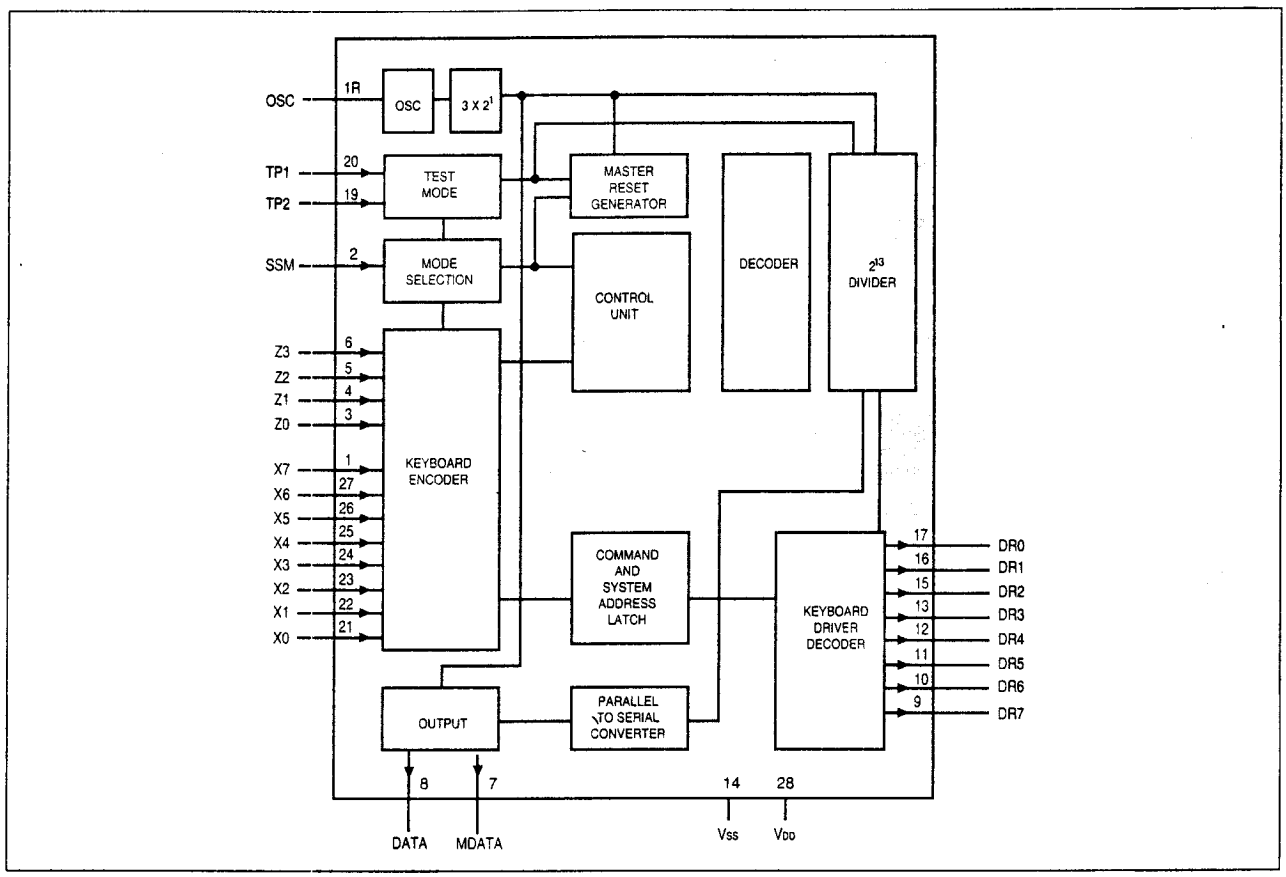
(1)General Description

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utiizes a keyboard with a single pole switch for each key. The commands ae arranged so that 32 systems can be addressed, each system containing 64 different commands.

(2) Features

- Low voltage requirement
- Single pin oscillator
- Biphase transmission technique
- Test mode facility

(3) Block Diagram



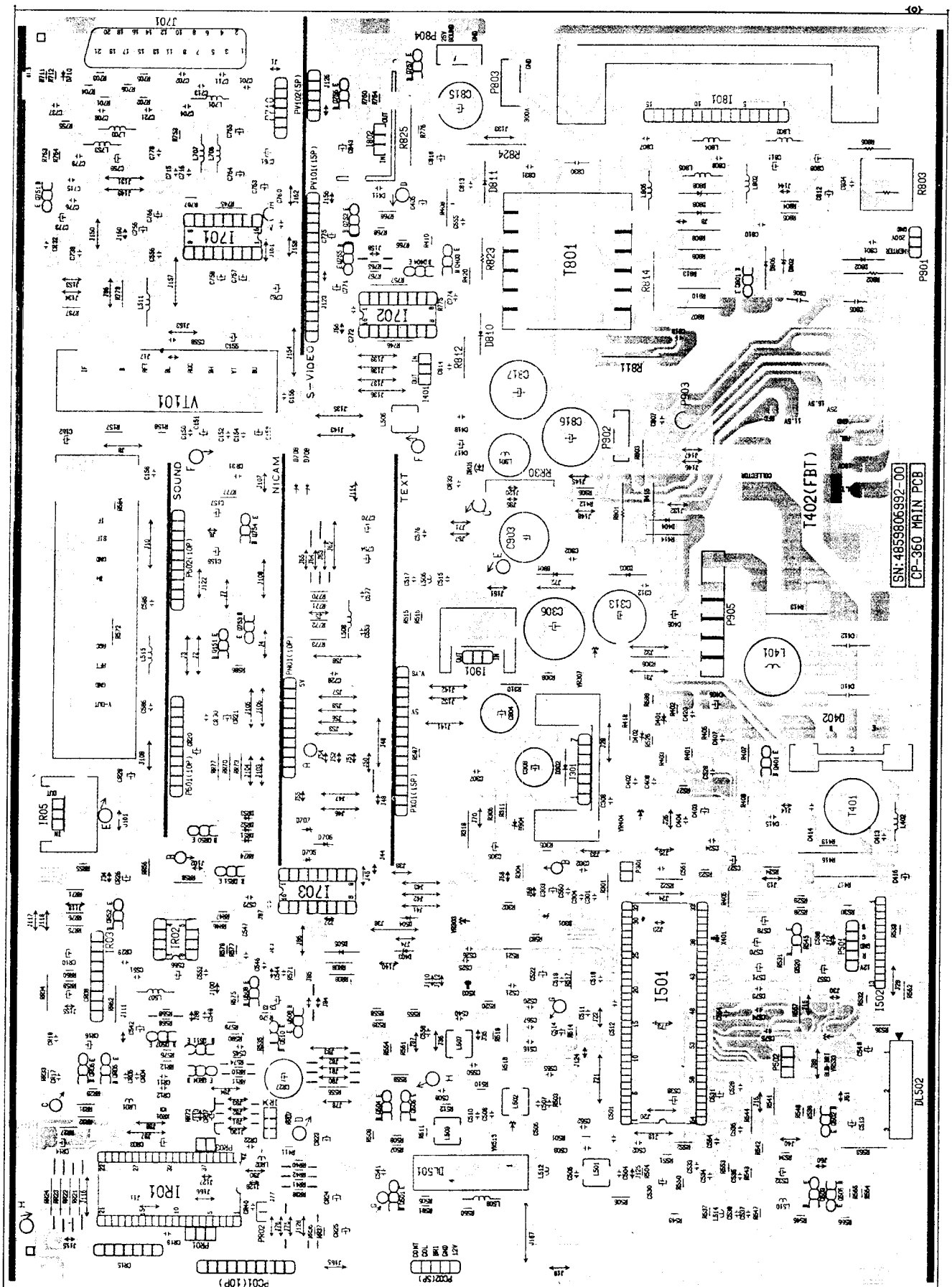
(4) Pin Description

Pin	Mnemonic	Function
1	X7 (IPU)	Sense input from key matrix
2	SSM (I)	System mode selection input
3-6	Z0-Z3 (IPU)	Sense inputs from key matrix
7	MDATA (OP3)	Generate output data modulated with 1/12 the oscillator frequency at a 25% duty factor
8	DATA (OP3)	Genarate output information
9-13	DR7-DR3 (ODN)	Scan drivers
14	Vss	Ground (0V)
15-17	DR2-DR0 (ODN)	Scan drives
18	OSC (I)	Oscillator input
19	TP2 (I)	Test point 2
20	TP1 (II)	Test point 1
21-27	X0-X6 (IPU)	Sense inputs from key matrix
28	VDD (I)	Voltage Supply

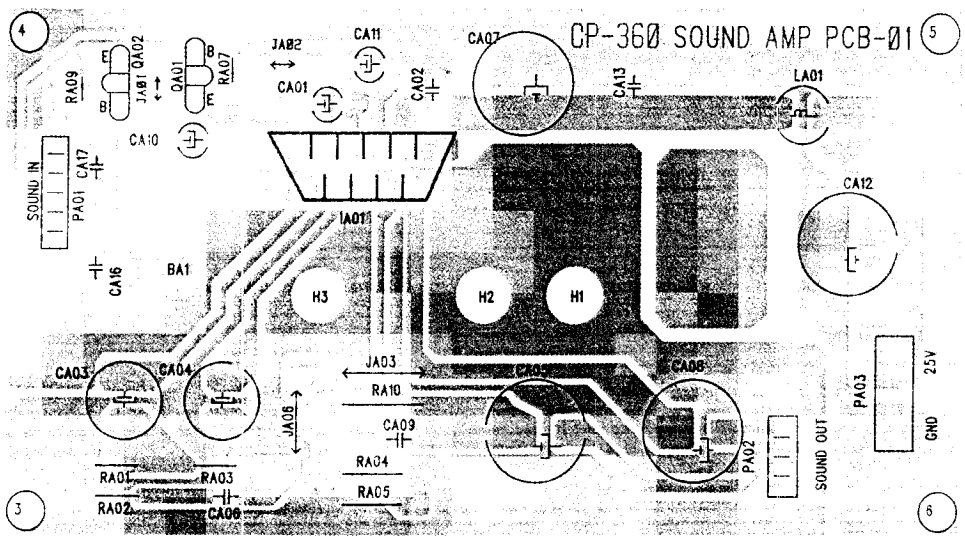
(I) = input
(IPU) = input with p-channel pull-up transistor
(ODN) = output with open drain n-channel transistor
(OP3) = output 3-state

PRINTED CIRCUIT BOARDS

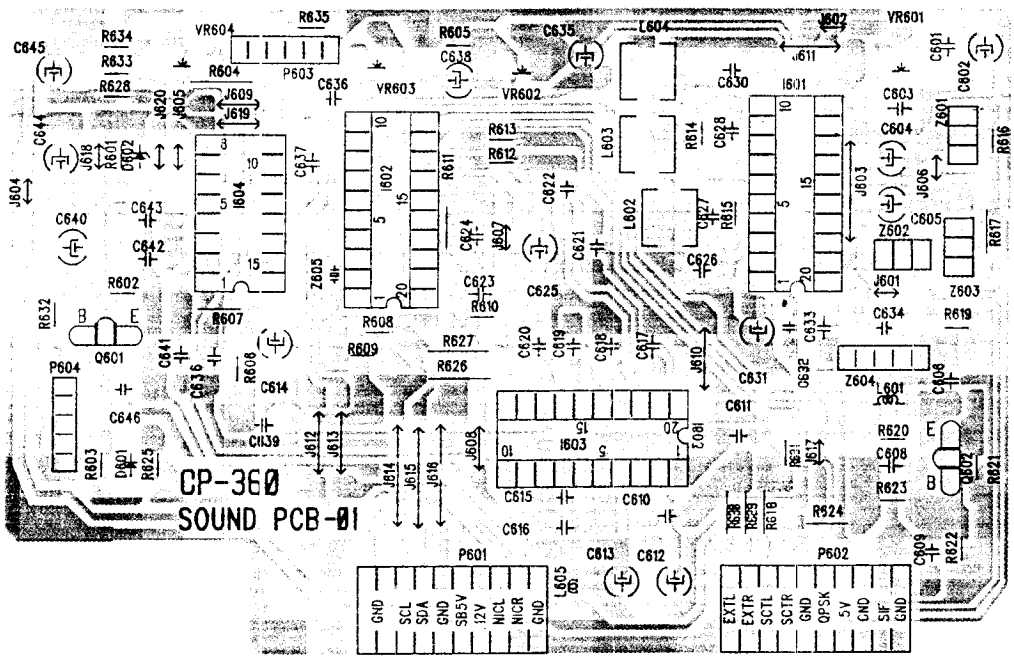
■ MAIN PCB- Solder Side-



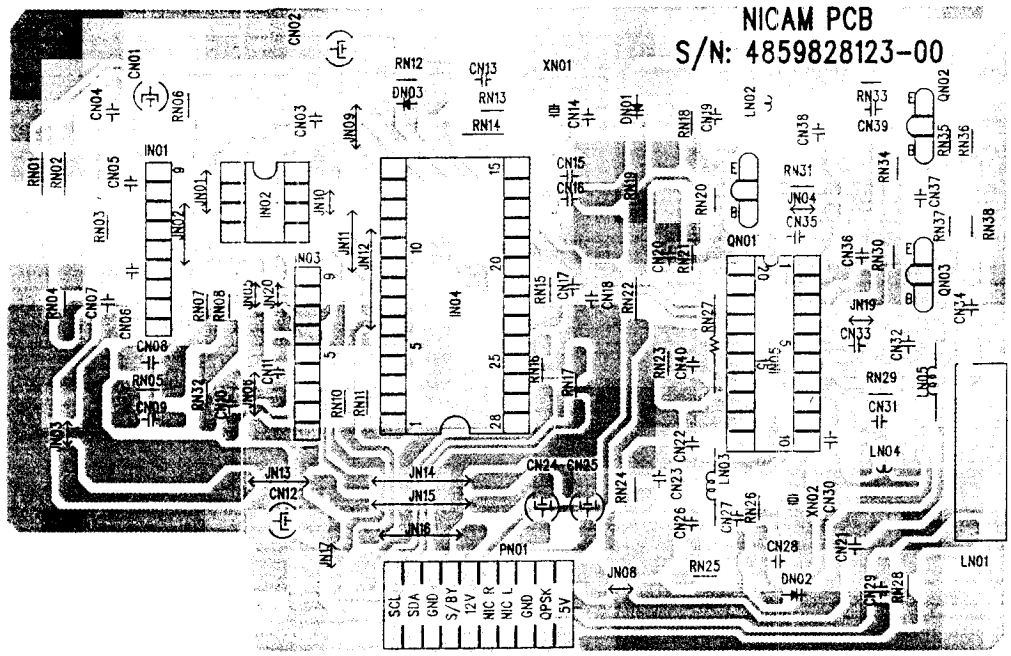
■SOUND AMP PCB -Solder Side-



■SOUND PCB -Solder Side-

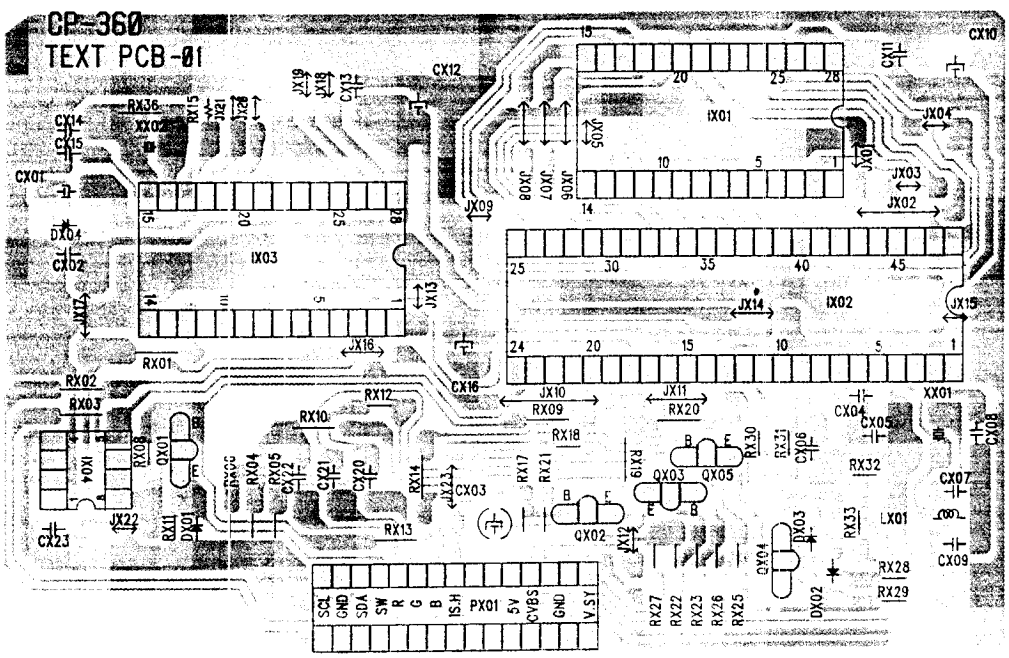


■NICAM PCB -Solder Side-

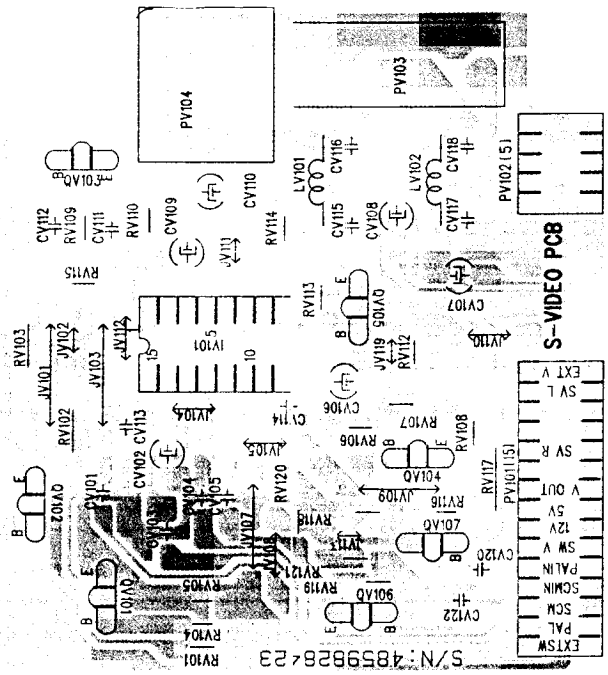


For Service Manuals Contact
MAURITRON TECHNICAL SERVICES
8 Cherry Tree Rd, Chinnor
Oxon OX9 4QY
Tel:- 01844-351694 Fax:- 01844-352554
Email:- enquiries@mauritron.co.uk

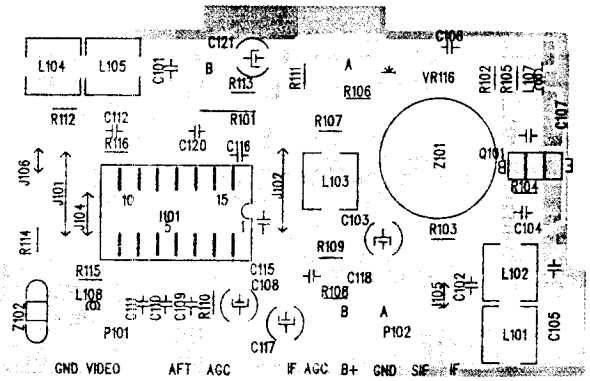
■TEXT PCB -Solder Side-



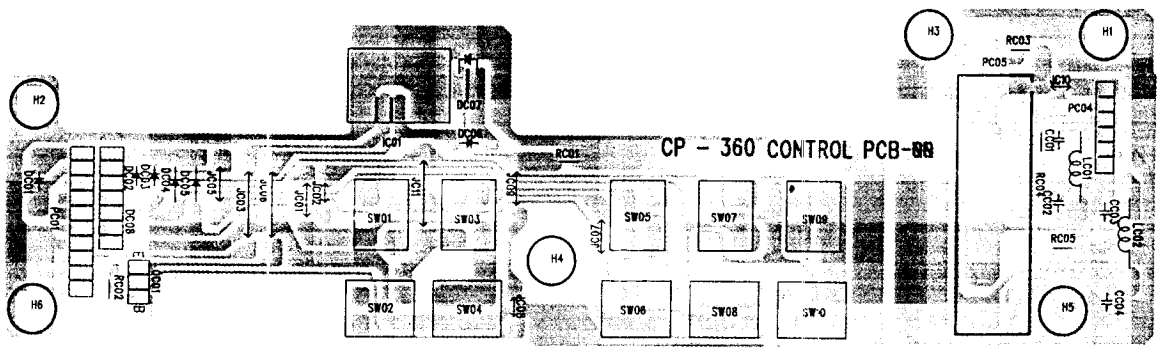
■S-VIDEO PCB -Solder Side-



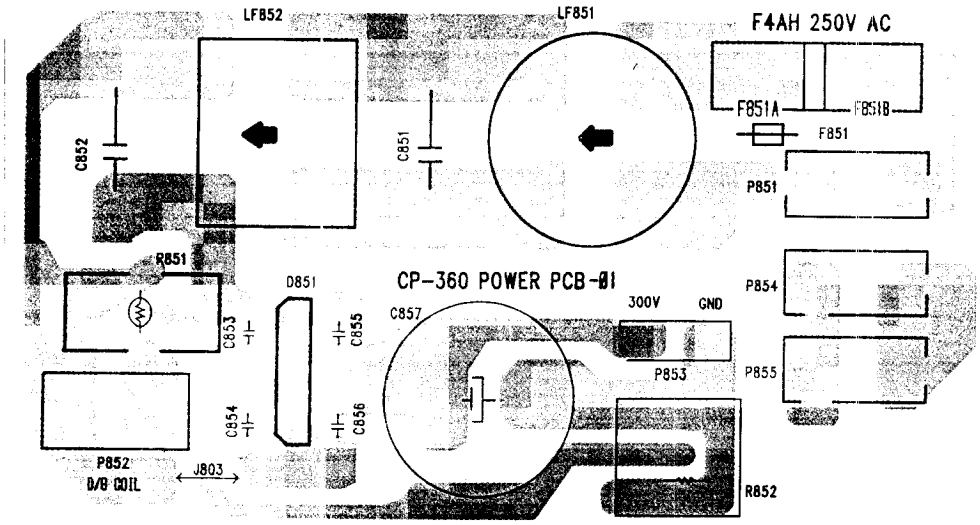
■IF PCB -Solder Side-



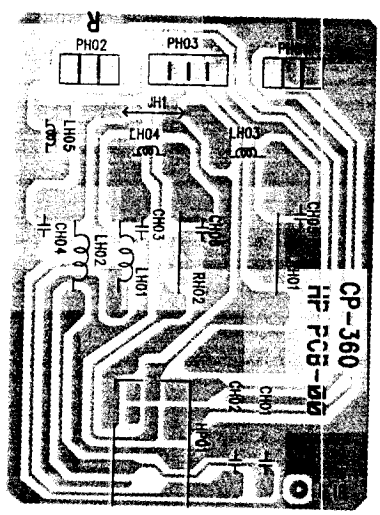
■CONTROL PCB -Solder Side-



■POWER PCB -Solder Side-



■HEAD PHONE PCB -Solder Side-



■CRT PCB -Solder Side-

For Service Manuals Contact
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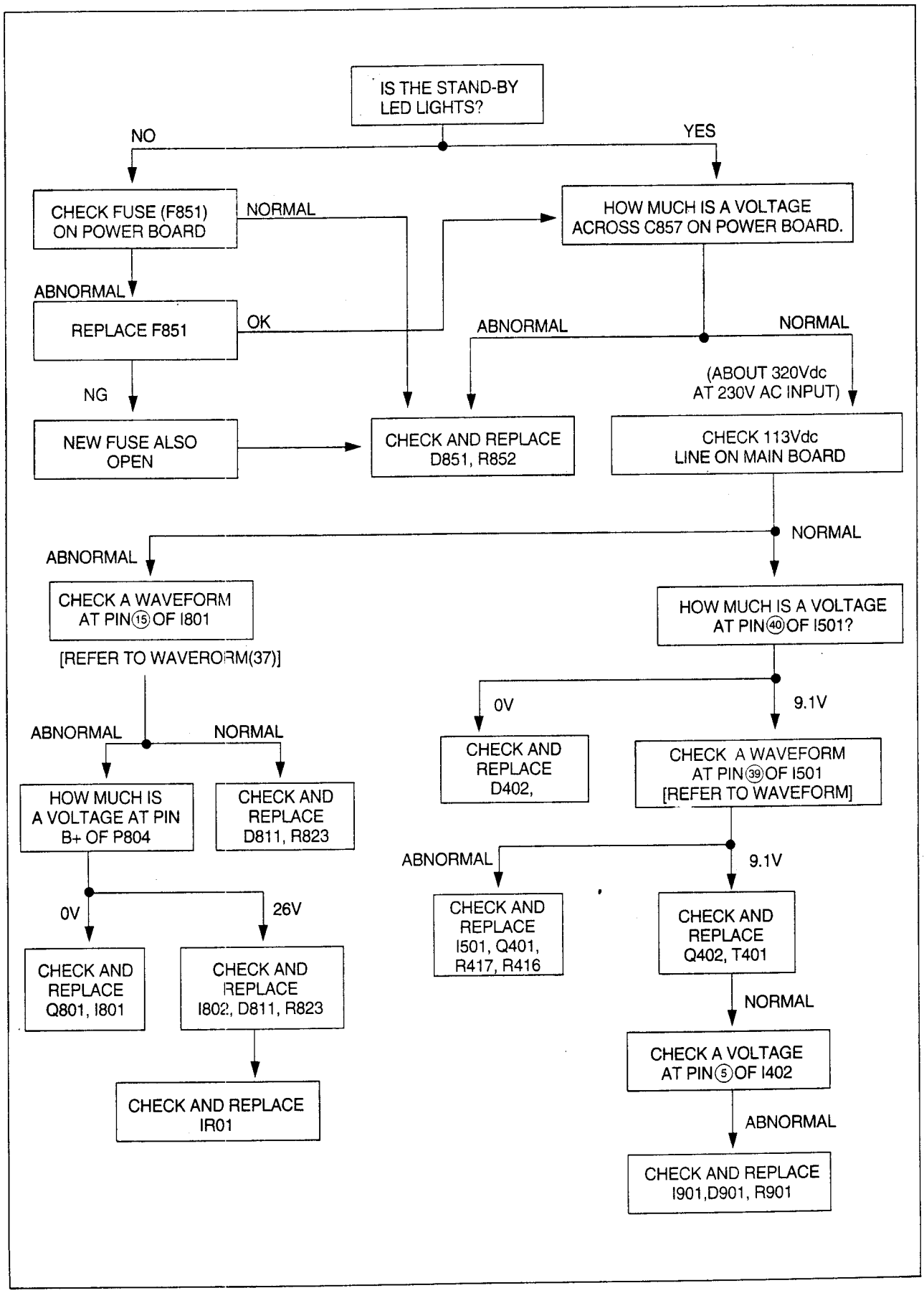
8 Cherry Tree Rd, Chinnor
Oxon OX9 4QY
Tel:- 01844-351694 Fax:- 01844-352554
Email:- enquiries@mauritron.co.uk

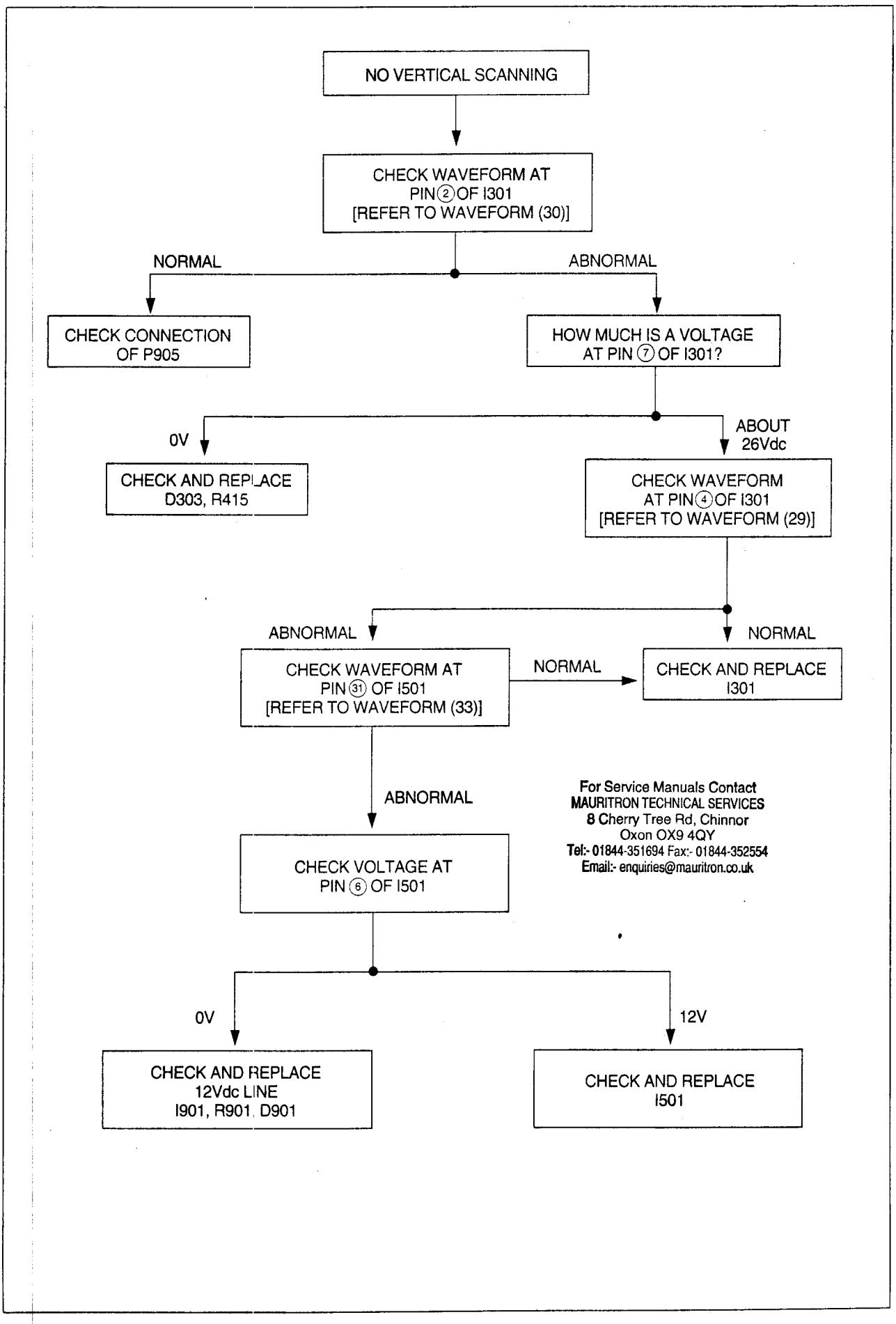
TROUBLE SHOOTING CHARTS

NOTE: In all process, the service-man must check all bias circuits that are related with each troubled part.

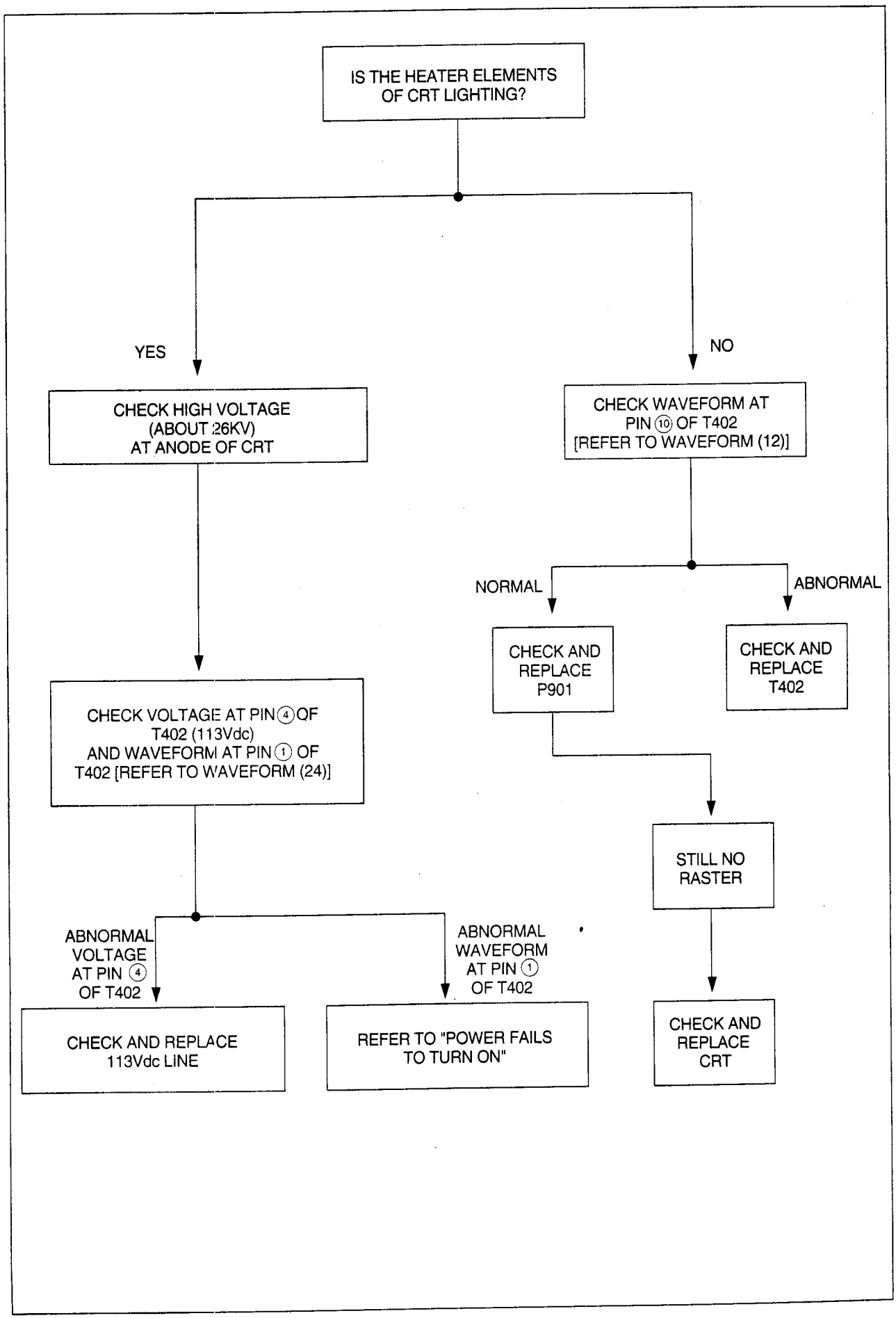
1. POWER FAILS TO TURN ON (NO PICTURE, NO SOUND, DOES NOT TURN ON)



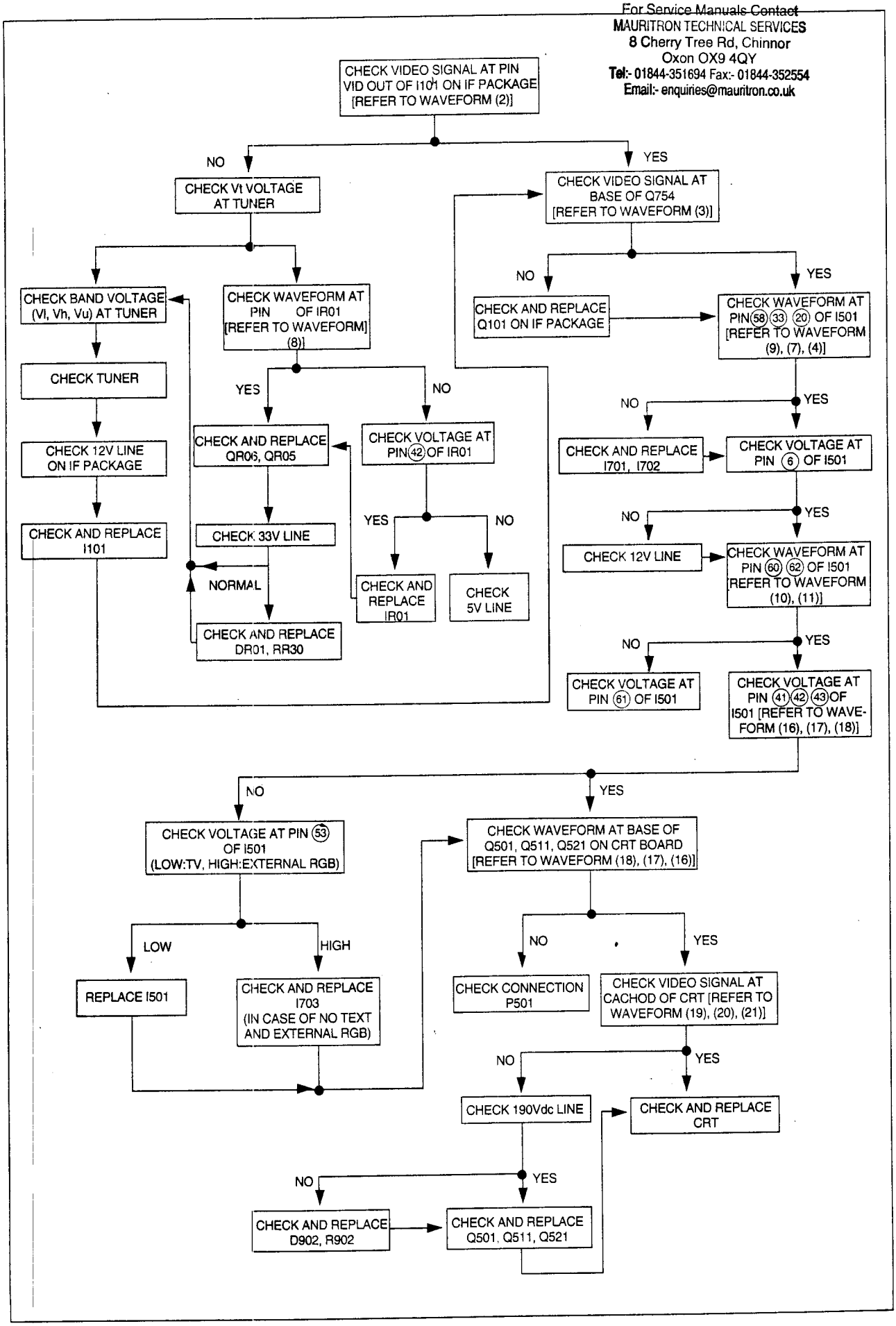
2. NO VERTICAL SCANNING



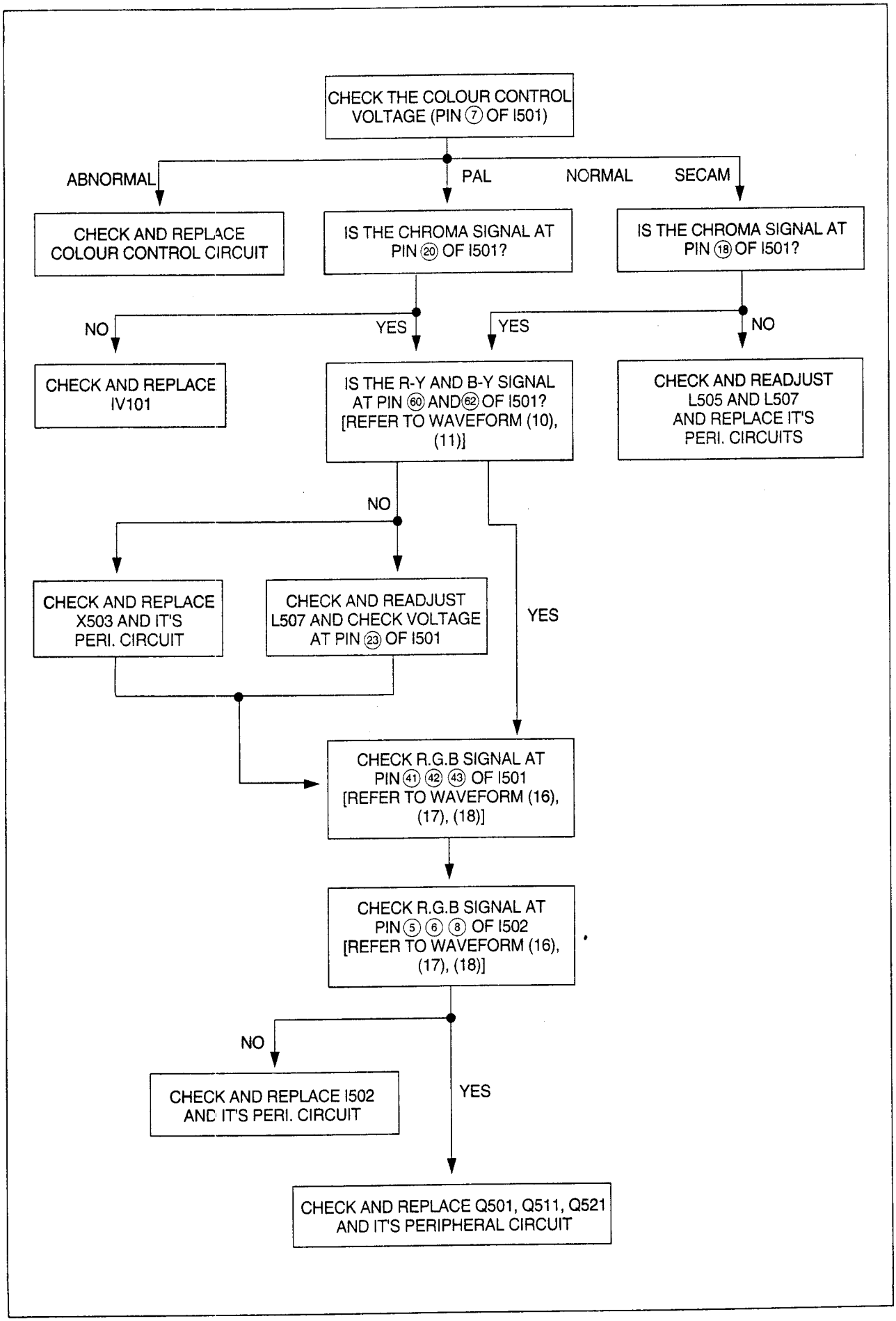
3. NO RASTER (SOUND OK)



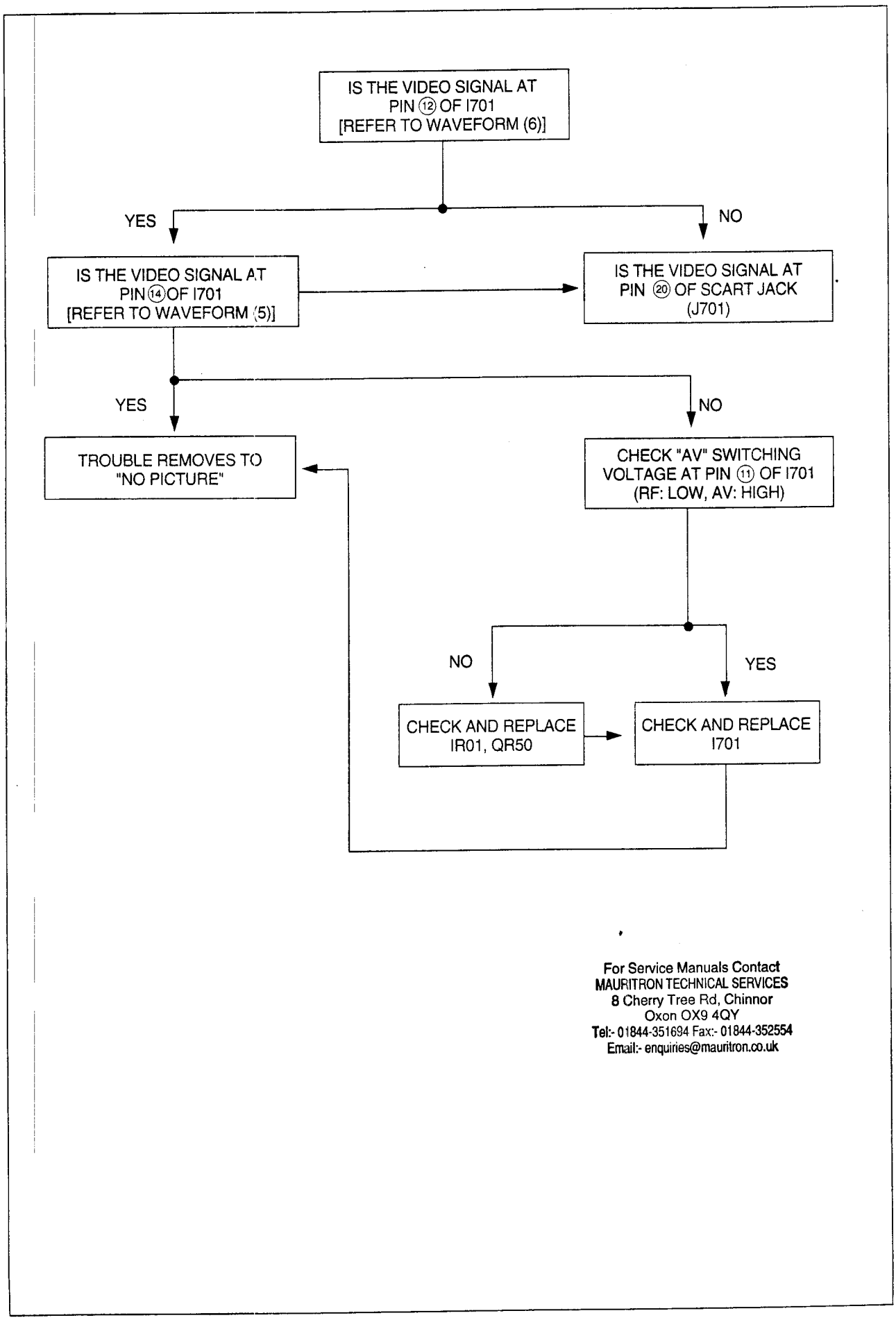
4. NO PICTURE (RASTER REMAINS, NO SOUND)



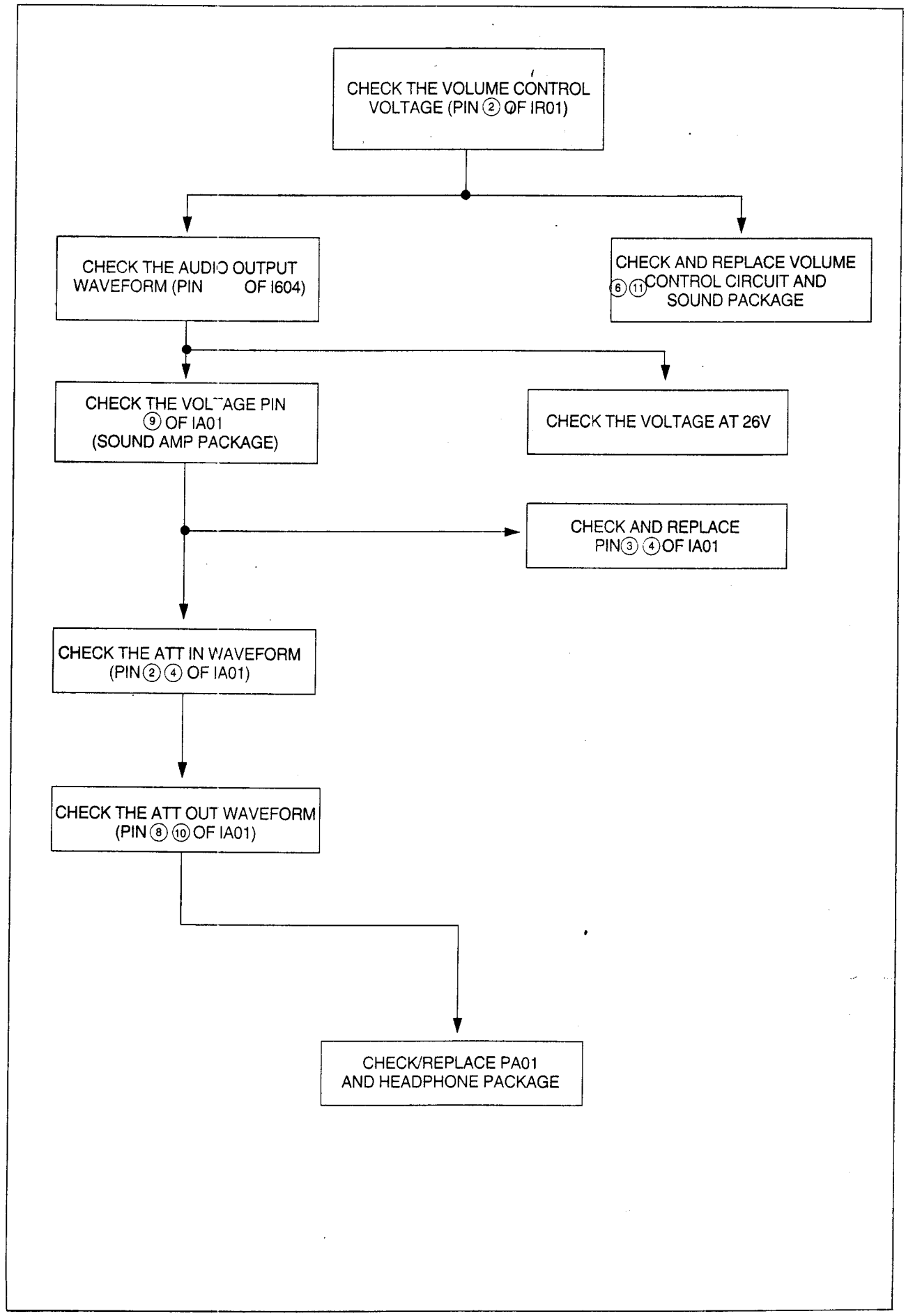
5. NO COLOUR


CHECK THE COLOUR CONTROL VOLTAGE (PIN ⑦ OF I501)
ABNORMAL
PAL
NORMAL
SECAM
CHECK AND REPLACE COLOUR CONTROL CIRCUIT
IS THE CHROMA SIGNAL AT PIN ⑳ OF I501?
IS THE CHROMA SIGNAL AT PIN ⑱ OF I501?
NO
YES
YES
NO
CHECK AND REPLACE IV101
IS THE R-Y AND B-Y SIGNAL AT PIN ⑥⓪ AND ⑥② OF I501? [REFER TO WAVEFORM (10), (11)]
CHECK AND READJUST L505 AND L507 AND REPLACE IT'S PERI. CIRCUITS
NO
CHECK AND REPLACE X503 AND IT'S PERI. CIRCUIT
CHECK AND READJUST L507 AND CHECK VOLTAGE AT PIN ㉓ OF I501
YES
CHECK R.G.B SIGNAL AT PIN ④① ④② ④③ OF I501 [REFER TO WAVEFORM (16), (17), (18)]
CHECK R.G.B SIGNAL AT PIN ⑤ ⑥ ⑧ OF I502 [REFER TO WAVEFORM (16), (17), (18)]
NO
YES
CHECK AND REPLACE I502 AND IT'S PERI. CIRCUIT
CHECK AND REPLACE Q501, Q511, Q521 AND IT'S PERIPHERAL CIRCUIT

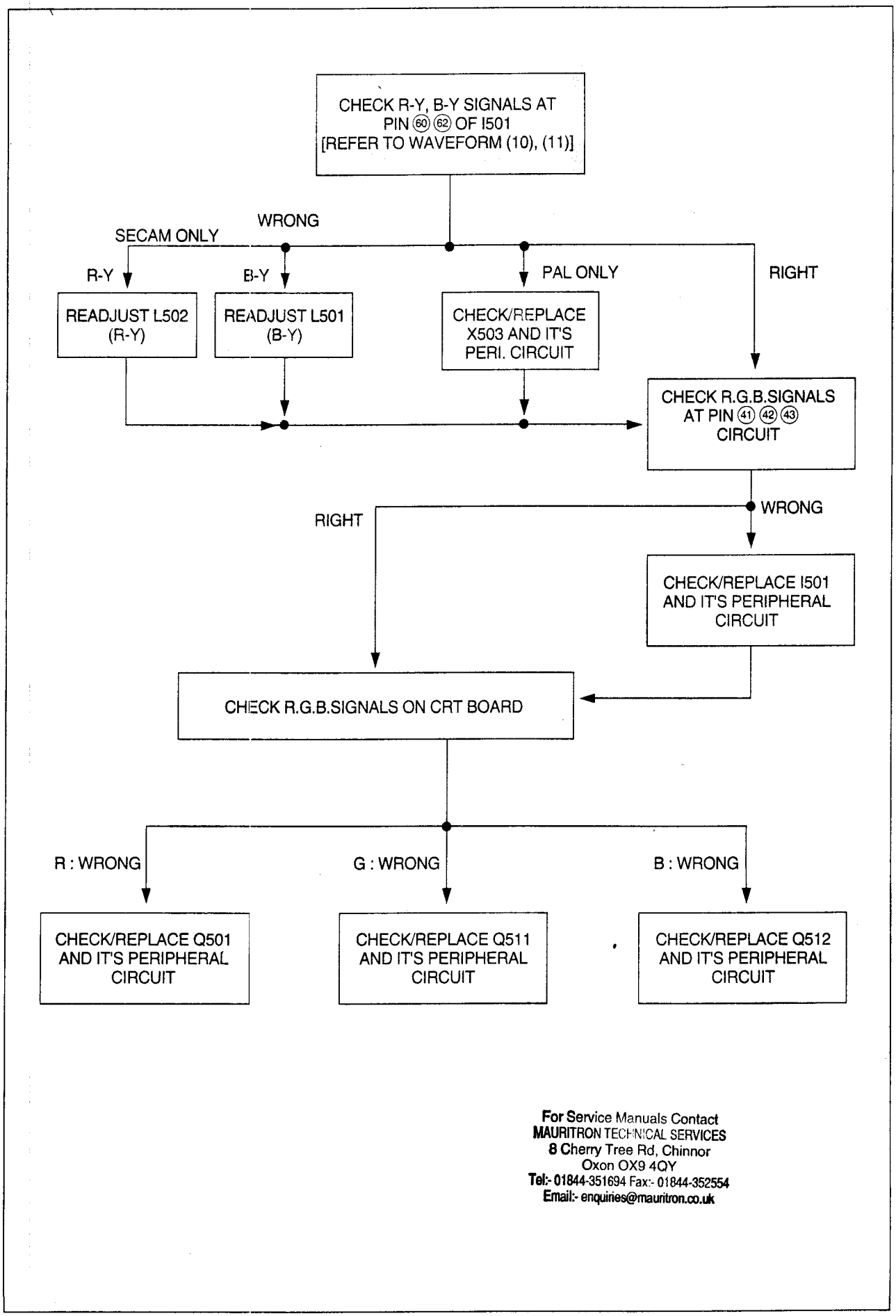
6. NO PATTERN (RF SIGNAL IS OK)



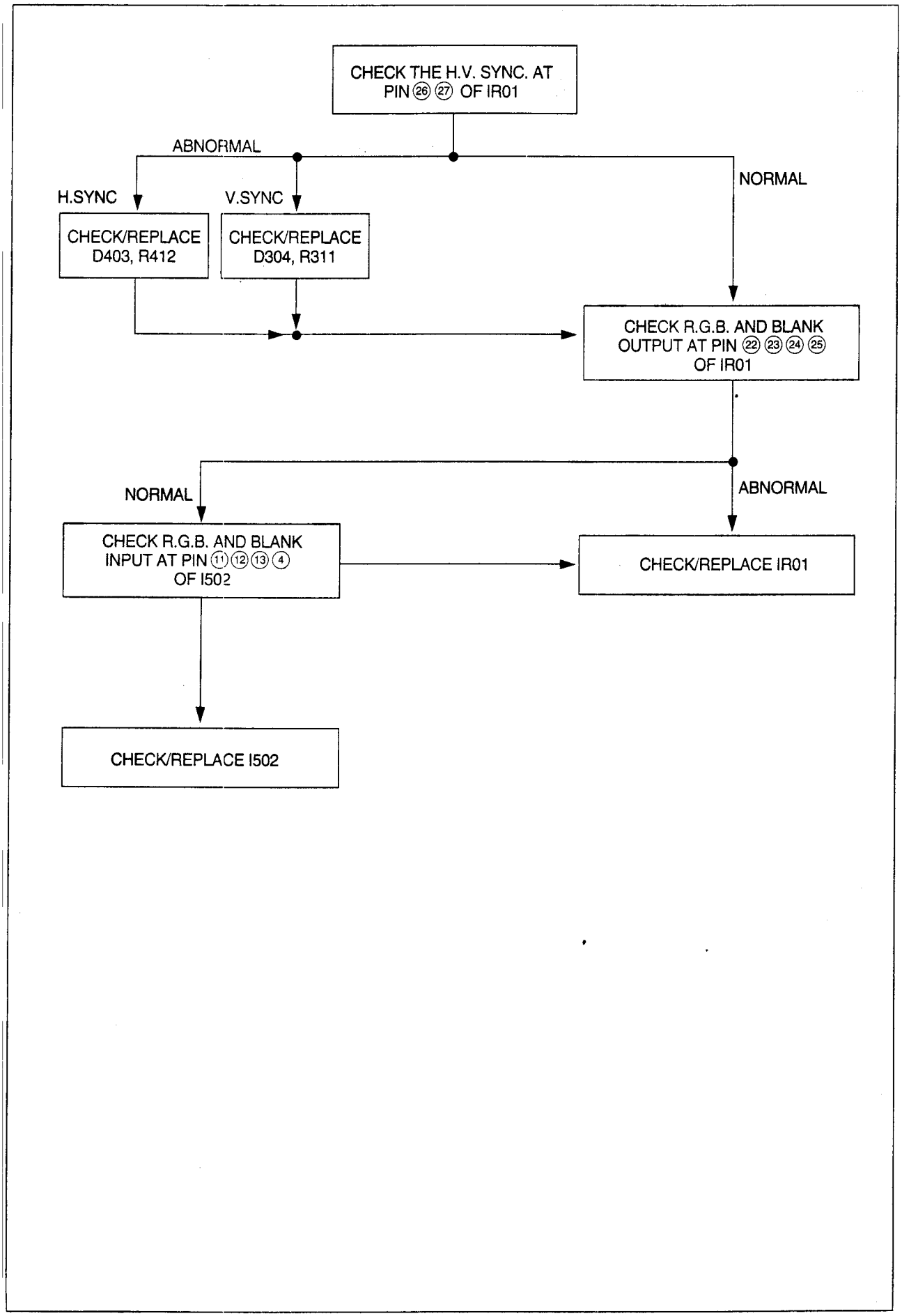
7. NO SOUND (PICTURE IS OK)



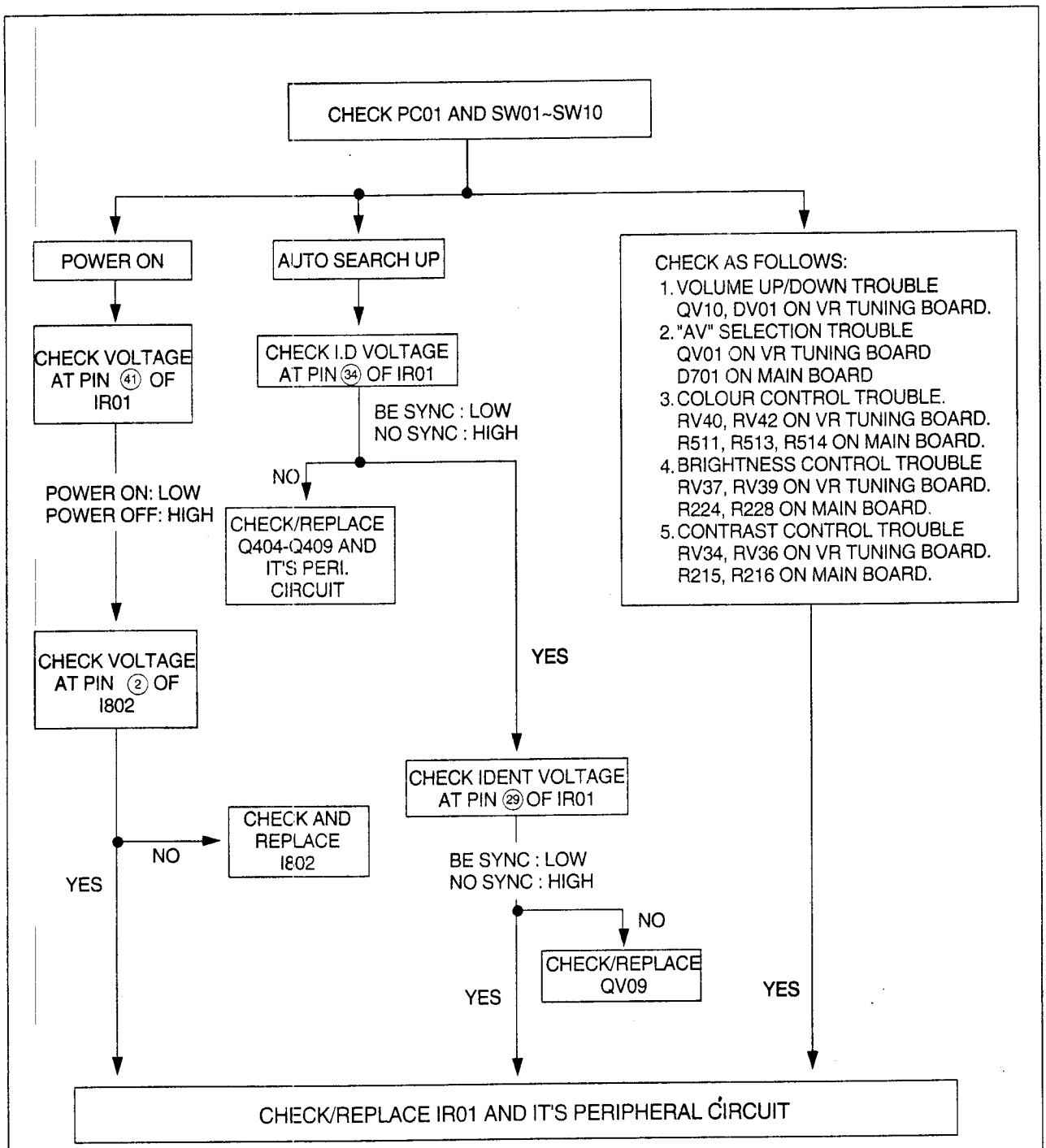
8. NO SPECIFIC COLOUR



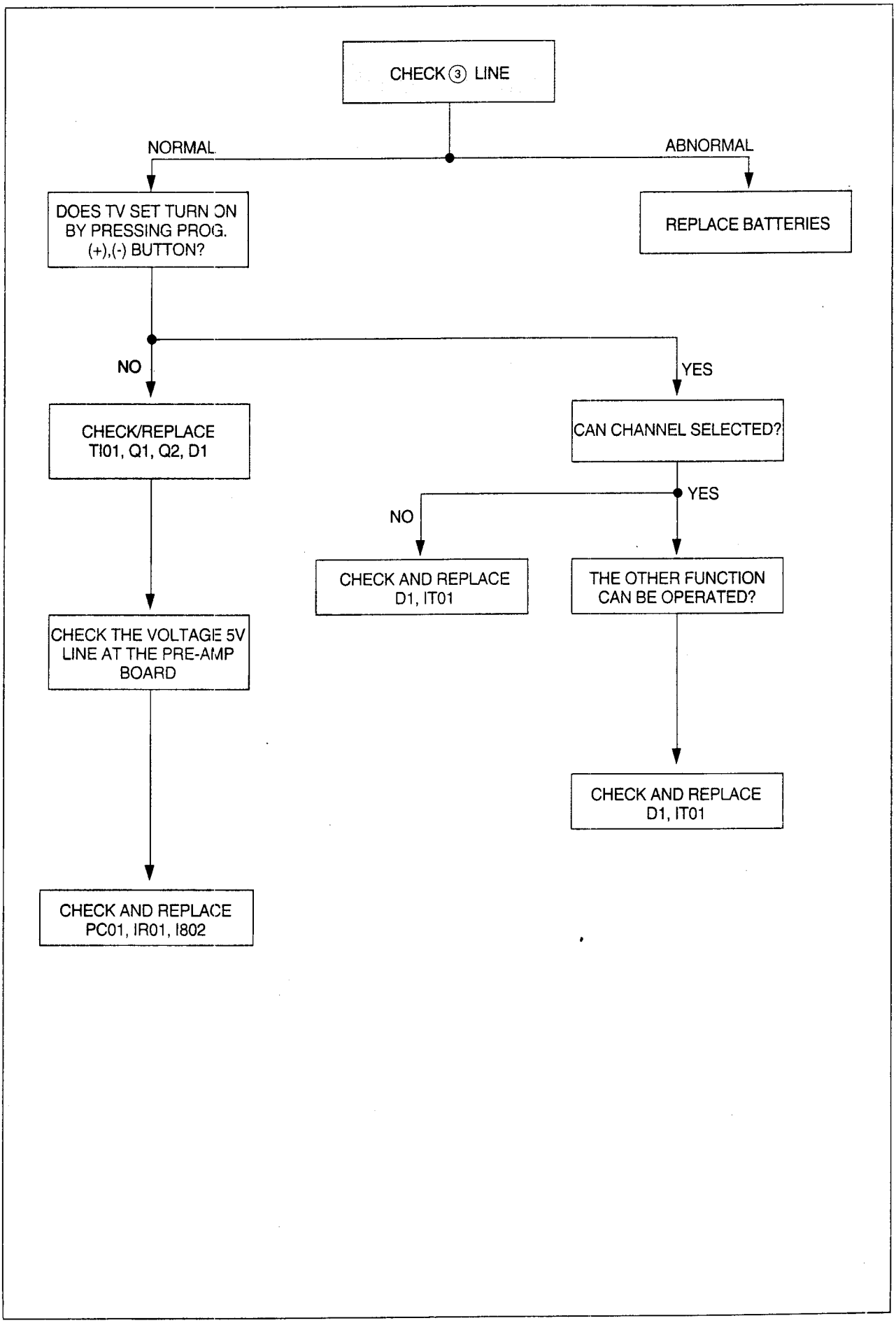
9. NO ON SCREEN DISKPLAY (PICTURE IS OK)



10. CONTRO SYSTEM TROUBLE



11. REMOCON IS NOT OPERATING



12. TEXT IS NOT OPERATING (PICTURE IS OK)